Design of the Digitizing Beam Position Limit Detector*

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Abstract. The Digitizing Beam Position Limit Detector (DBPLD) is designed to identify and react to beam missteering conditions in the Advanced Photon Source (APS) storage ring. The high power of the insertion devices requires these missteering conditions to result in a beam abort in less than 2 milliseconds. Commercially available beam position monitors provide a voltage proportional to beam position immediately upstream and downstream of insertion devices. The DBPLD is a custom VME board that digitizes these voltages and interrupts the heartbeat of the APS machine protection system when the beam position exceeds its trip limits.

INTRODUCTION

Insertion devices in the APS storage ring are powerful enough to damage the vacuum chamber in the event of a missteered beam. Beam position monitors that are located immediately upstream and downstream of insertion devices produce an analog signal proportional to beam position. Position signals are available from each BPM for both horizontal and vertical planes. These BPMs also generate signals that can be used to determine if stored beam is present and whether or not the BPM is functioning. The Digitizing Beam Position Limit Detector (DBPLD) samples the analog output of these BPMs and notifies the machine protection system (MPS) (1) if the beam is missteered. Once notified, the MPS will dump the stored beam by temporarily interrupting the rf system for 100 milliseconds. This paper describes the design of the DBPLD with specific attention to design methods and features that support reliable operation. The DBPLD was designed specifically to work with the commercially available Bergoz BPM

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(2), but is compatible with any device that can supply a voltage that is proportional to beam position.

ARCHITECTURE

The DBPLD is a 6U VME board that supports two separate insertion devices (IDs) and provides an interface to the Machine Protection System and EPICS (3), the APS control system. Figure 1 shows a diagram with DBPLD inputs and outputs.

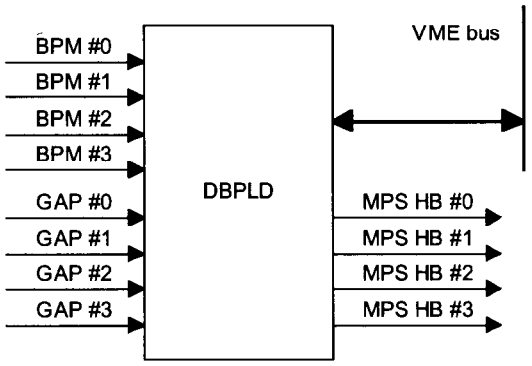

FIGURE 1. DBPLD inputs and outputs. One DBPLD board supports four BPMs that cover two insertion devices. Insertion device gap open/closed status is sensed through the GAP inputs. An optical heartbeat (MPS HB) is sent to the machine protection system when no missteering condition exists. The DBPLD is interfaced to the APS control system through an onboard VME interface.

Four BPM channels provide coverage for two IDs, with one BPM immediately upstream of an ID and one BPM immediately downstream. At the APS, IDs have redundant gap interlock switches that detect when the gap is fully open. The DBPLD is disarmed in this case. The four GAP interlock inputs on the DBPLD cover the two insertion devices. Four heartbeat (HB) connections allow the MPS to detect which of the four channels generated a beam abort.

The DBPLD has analog-to-digital converters (ADCs) at its front end, but is essentially a digital device. Internally, the DBPLD can be divided into three conceptual blocks: the datapath, the controller, and the VME interface/working RAM. These three sections communicate with each other over internal address, data, and control buses. A 5 MHz, board-wide clock drives every register on the board with the exception of the working RAM in the VME interface. The working RAM is a cycle-shared, dual-ported memory that requires a clock that runs at twice the frequency of the board-wide clock. Both of these clocks are derived from the same crystal and are in phase for fully synchronous operation. Throughout the system, data may only change at the rising edge of the board-wide clock. Asynchronous inputs run through registered synchronizers before they are sampled by the DBPLD. These and other techniques eliminate the hazards associated with metastability and provide robust, glitch-free operation.

A block diagram of the DBPLD is shown in Figure 2. Most of the detail shown is in the datapath. Data flows through the datapath under the direction of the controller. The VME interface doubles as a board-wide working memory where data can be stored and retrieved. This memory is dual ported, with the VME interface on one side and the

datapath on the other. This architecture allows the APS control system full monitoring capability of DBPLD operation. With a mechanical key inserted in the DBPLD front panel, the control system may also write to the working memory through the VME interface.

DATAPATH

At the front end of the datapath are eight analog-to-digital converter sections, one for each channel and plane. These sections consist of a low-cost, eight-bit analog-to-digital converter coupled with a support circuit. The support circuit triggers the ADC and synchronizes its data to the DBPLD board-wide clock. A block diagram showing the support circuit and its relationship to the ADC and the DBPLD internal buses is shown in Figure 3.

The ADC requires 30 μs to make an analog-to-digital conversion, but it is only triggered once every 51.2 μs. Compare these times to the 200 ns period of the board-wide clock. The clock runs many times faster than the ADC conversion cycle. The support circuit simplifies the architecture by hiding the slower ADC from the rest of the design. A register in the support circuit stores the last valid output of the ADC for immediate transfer on the data bus any time it is addressed. This means that other parts of the circuit do not need to worry about accessing the ADC in the middle of a conversion, since data is always valid at the output of the support circuit. This method insures that the data bus is never driven with partially latched data.

Each of the eight analog to digital converter sections shares a common tri state data bus, address bus, and control bus. These shared buses run throughout the DBPLD and allow a simple time division multiplexed datapath to be used. Data flows from inputs at the top edge of Figure 2 to outputs on the bottom edge. The controller directs data on their way through the datapath with signals on the control and address buses. Notice that the data bus does not connect to the controller.

Analog signals that are delivered to the front panel of the DBPLD originate from BPMs that can be several feet away. These signals are transmitted over cables that could possibly become disconnected. A disconnected cable must generate a fault and cause a beam abort. The clock signal from the commercial BPM is shipped out over the same cable as the position data. Watchdog timers on board the DBPLD monitor clock signals from each BPM. These watchdogs look for changes in state of the BPM clock and assert an alarm if the clock gets stuck in any particular state. If a cable is disconnected, the watchdog senses a non-changing state and raises an alarm. This mechanism also detects failures at the BPM, such as loss of power. There are four watchdogs, one associated with each channel. Each is addressable by the controller over the address bus.

Two other external signals are brought in through the front panel. They are insertion device gap open/closed status and beam present/not present. The DBPLD is armed only when the gap status is closed and when beam is present in the APS storage ring. ID gap status and beam status bits exist for each channel and are address selectable by the controller.

The DBPLD supports four BPMs or eight planes, four horizontal and four vertical. Each plane may have unique upper and lower trip limits. This means that there are two limits associated with each plane. The DBPLD retrieves the upper and lower limits from its working RAM one at a time and places them in the "high" and "low" datapath registers. It places the most recent beam position data associated with these limits in the "live" datapath register and at the same time writes this position data to a unique location

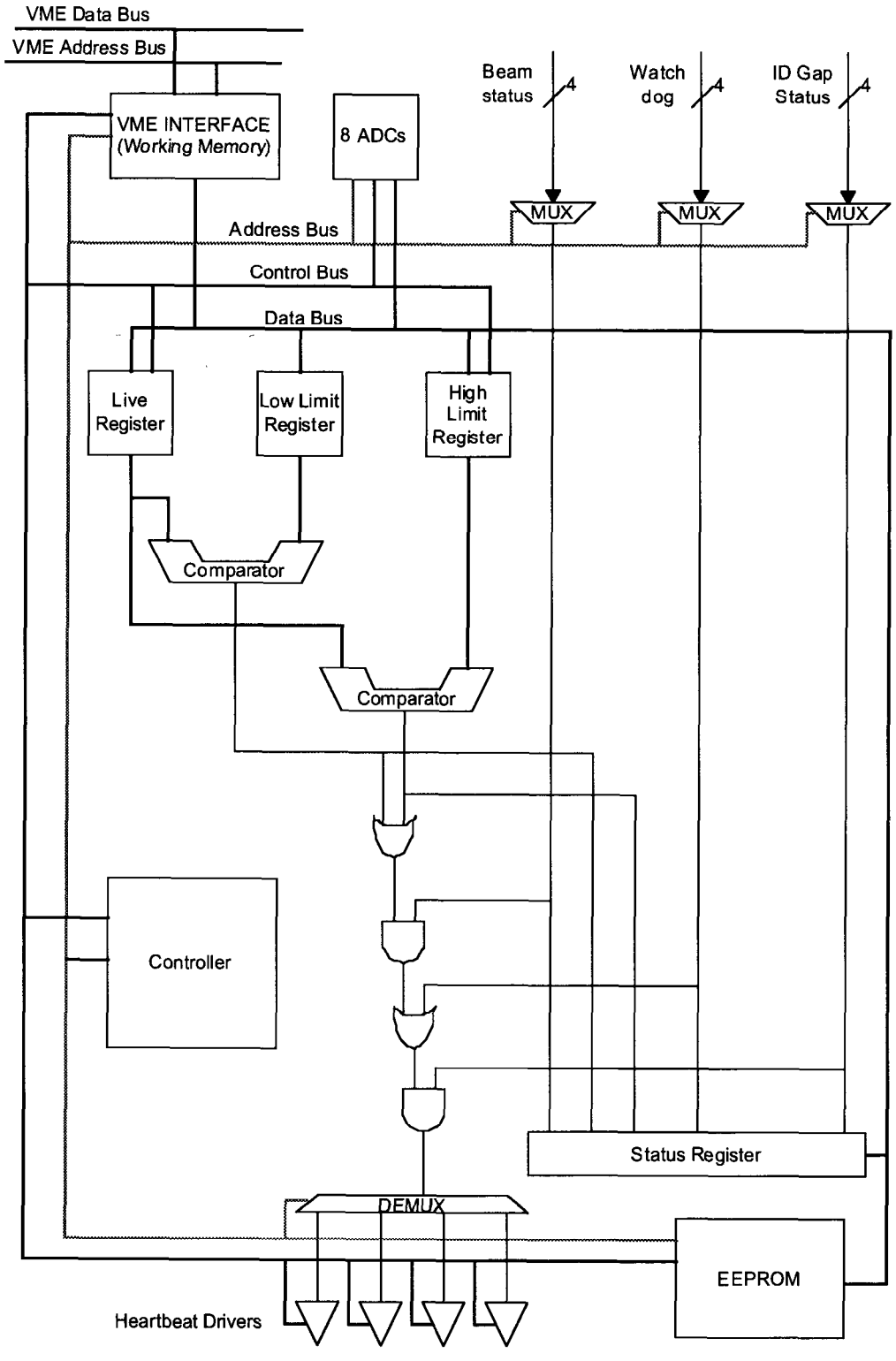

FIGURE 2. Block diagram of DBPLD internals.

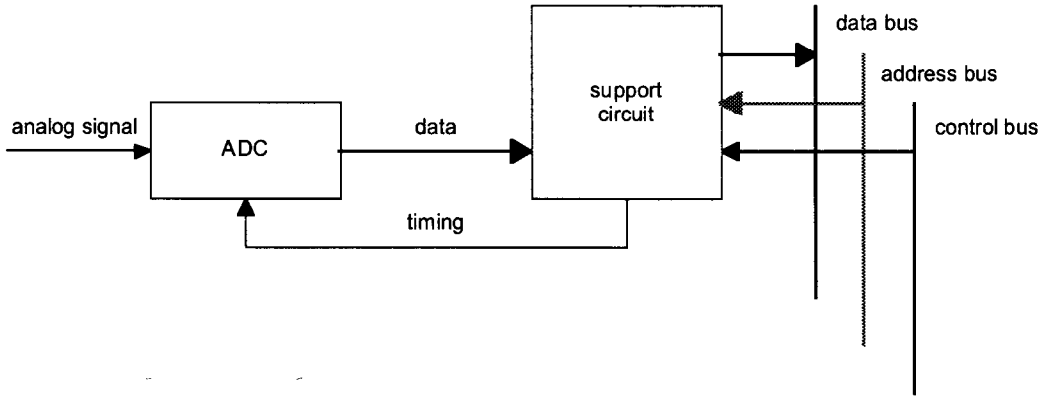

FIGURE 3. ADC section, analog-to-digital converter with support circuit. The support circuit simplifies timing between the ADC and the rest of the DBPLD.

in the working memory. The position data are compared with the high and low limits simultaneously by the two comparators. Combinational logic examines ID gap, beam present, and watchdog status and generates a heartbeat stop pulse, if necessary. The status register latches these signals. The contents of the status register are then stored to the appropriate working memory location. Since the working memory is dual ported with the VME interface, this mechanism allows the APS control system to access status, position, and limit information for all eight planes at any time.

A heartbeat generator is provided for each of the four channels. The heartbeat generators each supply a 1 MHz optical signal to the machine protection system. Absence of the 1 MHz signal indicates that a beam position limit has been exceeded or that there has been a fault on that channel. The machine protection system causes a beam abort when the heartbeat is absent.

During maintenance periods at the APS, VME crates are often powered down for service. To prevent limit settings from being lost under these circumstances, an electrically erasable-programmable read only memory (EEPROM) is used. When new trip limits are written to the VME interface from the EPICS-based control system, a dirty bit is set. The controller watches for this dirty bit and commits newly written limits to the EEPROM and then clears the dirty bit. At power up, limits are read out of the EEPROM.

CONTROLLER

Information on the internal address and control buses originates from the controller. The controller is a finite-state machine that is implemented in programmable logic using a hardware description language. Data flows through the datapath, but it is the controller that directs this flow.

At power up, the DBPLD enters an initialization mode where it loads the system RAM with limits from the EEPROM. When completed, it begins limit-checking operation. In the limit-checking mode, the DBPLD controller cycles through ten repeating states. These ten states constitute a minor cycle in which one of eight positions is compared against its trip limits. When the minor cycle completes eight times, a major cycle has been completed. Both horizontal and vertical positions for all four channels are

checked during a major cycle. In Figure 4, the ten states are abstracted as five steps, with a distinct task completed in each step. The variable, m, denotes the minor cycle number and can range from 0 to 7. The table on the right side of the figure indicates the focus for any particular minor cycle. The address counter rolls over to 0 automatically after reaching a value of 31 so that major cycles repeat without any special action by the controller.

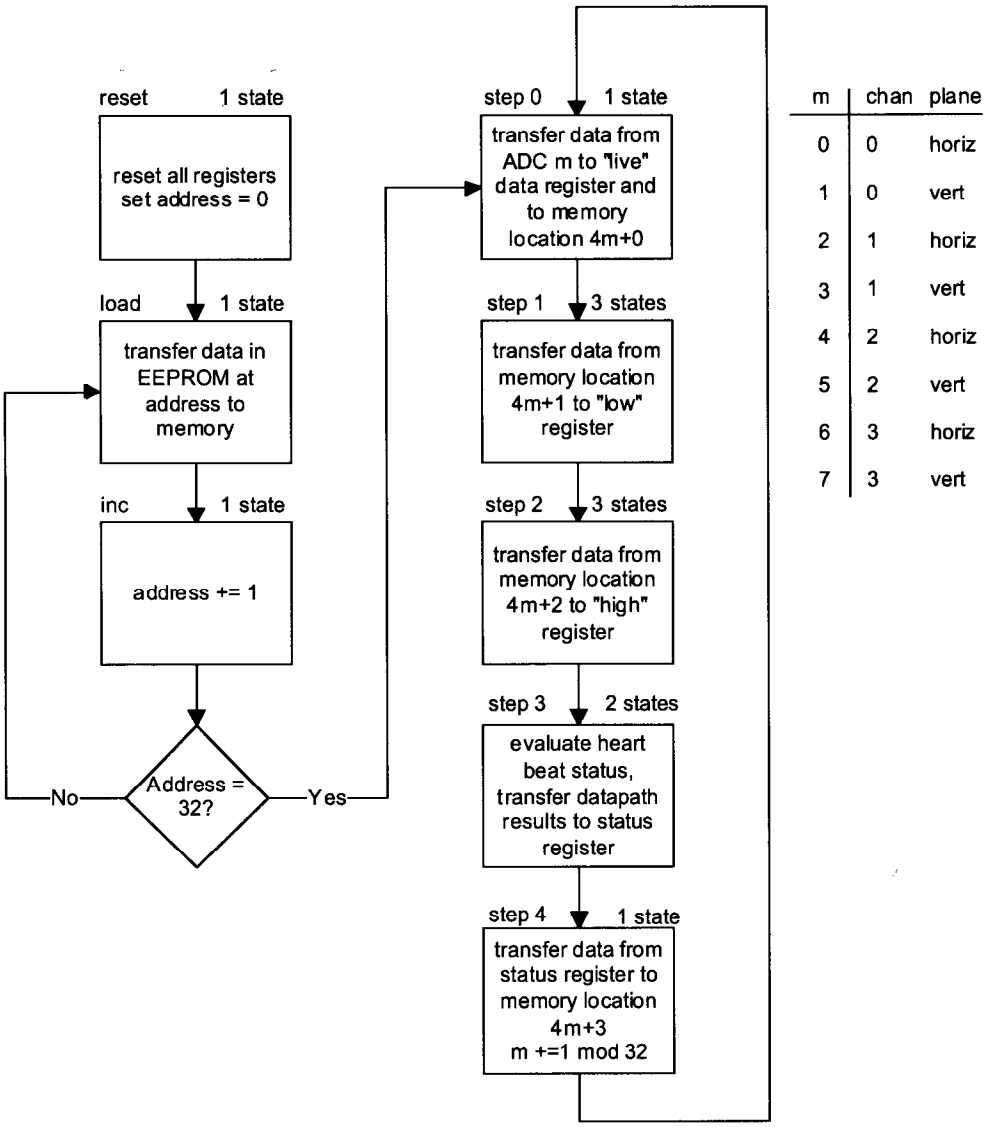

FIGURE 4. Controller state diagram.

RESPONSE TIME

The board-wide clock runs at 5 MHz, corresponding to a clock period, t_{clock}, of 200 ns. The time for one minor cycle to complete, t_{minor}, is computed as

$$t_{minor} = t_{clock} \times N = 200ns \times 10 = 2\mu s, \quad (1)$$

where N is the number of clock periods required for a minor cycle. The time for one major cycle to complete, t_{major}, is computed as

$$t_{major} = t_{minor} \times M = 2\mu s \times 8 = 16\mu s, \quad (2)$$

where M is the number of minor cycles in every major cycle. According to Equation (2), the DBPLD completes a major cycle every 16 µs.

The response time of the DBPLD is limited by the 51.2 µs conversion time of the ADC section, t_{ADC}. Two conditions must be met for the DBPLD to respond in this minimum amount of time. First, the change at the input must occur immediately before the ADC receives a convert pulse. Second, the ADC support circuit has to latch this sample on the clock cycle immediately before the controller transfers that same data to the "live" register. The maximum or worst-case response time results when the step in the input occurs during an ADC conversion cycle and the controller has just finished examining data from that ADC. In this case, two full conversion cycles and a major cycle of the state machine must take place. The worst-case response time, $t_{response}$ is computed in Equation (3):

$$t_{response} = t_{major} + 2 \times t_{ADC} = 16\mu s + 2 \times 51.2\mu s = 118.4\mu s. \quad (3)$$

Measurements of best-case and worst-case response times are shown in Figure 5. The worst case measured time is slightly better than the calculated worst-case time. It is possible that the ADC can tolerate some change at the input immediately after the conversion cycle begins.

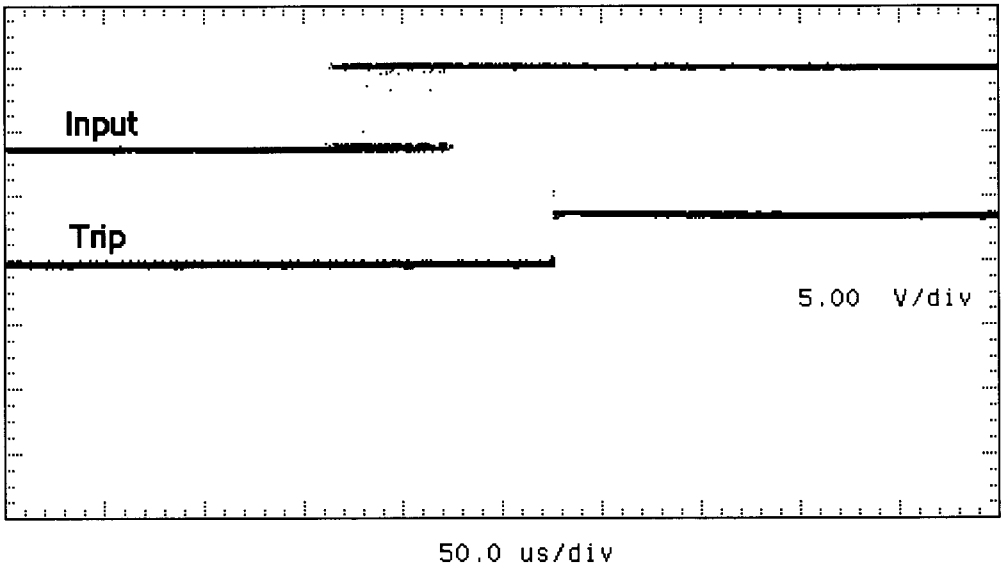

FIGURE 5. Response time measurement with a step input. The measurement shows a best case of 52 µs and a worst case of 113 µs. The figure shows 500 traces overlaid.

There is also a step response time associated with the BPM that supplies the position signal to the DBPLD. In the case of the Bergoz BPM, it is 580 μs. The end-to-end response time is then the sum of the BPM and DBPLD response times, which is less than 700 μs.

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