Beam Position Monitors for the Fermilab Recycler Ring

E. Barsotti, S. Lackey, C. McClure, R. Meadowcroft

Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

Abstract. Fermilab's new Recycler Ring will recover and cool "used" antiprotons at the end of a Tevatron store and also accumulate "new" antiprotons from the antiproton source. A wideband rf system based on barrier buckets will result in unbunched beam, grouped in one to three separate partitions throughout the ring. A new beam position monitor system will measure position of any one partition at a time, using low-frequency signals from beam distribution edges. A signal path including an elliptical split-plate detector, radiation-resistant tunnel preamplifiers, and logarithmic amplifiers, will result in a held output voltage nearly proportional to position. The results will be digitized using Industry Pack technology and a Motorola MVME162 processor board. The data acquisition subsystem, including digitization and timing for 80 position channels, will occupy two VME slots. System design will be described, with some additional emphasis on the use of logamp chips.

INTRODUCTION

Fermilab's Recycler Ring will be an 8 GeV storage ring constructed of permanent magnets (1). It will increase Tevatron collider luminosity in two ways. First, "used" antiprotons at the end of a store will be "recycled" and cooled in the Recycler. Also, accumulator high antiproton production rate will be maintained by periodically sending its stack to the Recycler for storage. The entire project was a late addition to the Main Injector project, funded with contingency money. The resulting time and money constraints played a role during subsystem development.

Besides the task of orbit measurement, the Beam Position Monitor system will be used for ion clearing. In fact, this dominated the decision to use two BPM detectors per half-cell, or 414 BPMs for the 3320-meter ring. The associated beamlines have an additional 32 BPMs. A cost-saving move briefly considered was to instrument only half the detectors.

The Recycler will have up to three partitions of beam at a time: cooled, warmer, and injected beam. These partitions will be separated by six "barrier buckets"created by the wideband rf system. No other rf will be used to modulate the beam, so the roughly 1 μs beam distribution edges at the barrier buckets will produce the only signals for BPM processing. This necessitates good low-frequency sensitivity, which, in turn, requires a high termination impedance and preamplifier near the detector. The rest of the processing chain is based on logarithmic amplifiers, or "logamps," before a timing module and commercial digitizers.

TUNNEL ELECTRONICS

The preamp and its associated circuitry reside in a metallic rf box, mounted on the base of the detector stand at the tunnel ceiling. Short coaxial cables and an additionalial grounding strap connect the box and the detector. The 0.3 m-long elliptical split-plate detectors match the Recycler beam pipe shape, with axis dimensions 96 mm by 44 mm. Particularly over the inner half-aperture, the vertical and horizontal detectors provide a nearly linear response to beam displacement, 0.32 and 0.7 dB/mm, respectively. Orthogonal transverse plane dependence is insignificant.

The parallel combination of detector and cable capacitance and termination resistor determine the low-frequency corner in a high-pass filter model of the detector (2). Setting that frequency (and resistor) involved a tradeoff. It must be high enough so that the signal from one beam partition decays before the next, to prevent interference. The anticipated gap between beam partitions is 1-2 μs. Too high a corner, however, decreases signal strength and decay rate unnecessarily. A simulation program was written to determine the optimal low-frequency corner of 300 kHz. Signal-to-noise optimization set a lowpass filter corner at 2 MHz. A shunt 50 MHz low-pass filter to 100 Ω was added to improve beam impedance at higher frequencies. Figure 1 shows actual detector and preamp response to a simulated beam signal. The analog processing focuses on the decaying signal, so matching the falltimes of the two plate signals is important.
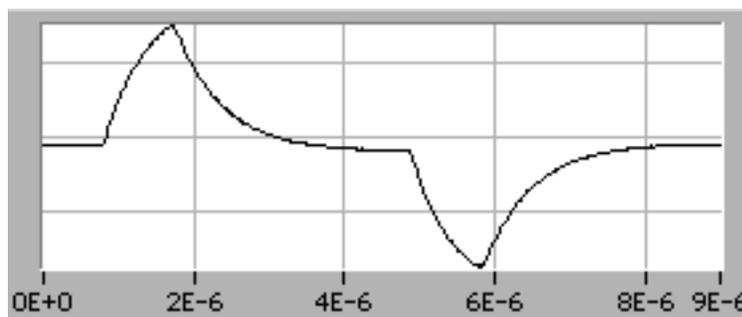
FIGURE 1. Response of a detector and preamp module to simulated beam signals.

A capacitive detector model is used here, since the detector is terminated with high impedance at the preamp. Above the corner frequency, signal strength on the detector is determined by:

$$V_c(t) = \frac{l\, I_b(t)}{2C_{tot}\, \beta_b\, c}, \quad C_{tot} = C_{det} + C_{cable}\ , \tag{1}$$

for detector capacitance C_{det}= 60 pf, cable capacitance C_{cable}= 40 pf, detector length l = 0.3 m, $\beta_b \approx 1$ for relativistic beam, and beam current $I_b(t)$= 10 mA for accumulator transfers of 10^{11} antiprotons. This represents the lower limit for beam current, with a maximum roughly 40 times higher. Position variation within a practical region of detector aperture causes signal ratios within ±10 dB. Adding the effect of the 300 kHz corner frequency, the preamp will handle a peak input voltage range of 21 mV to 2.4 V.

While radiation resistance is not a major concern throughout most of the ring, local "hot spots" due to the underlying Main Injector accelerator dictate the choice of preamp circuitry. These locations will reach up to 5 MRad/year, but this dosage is reduced by an estimated factor of 5 by shielding from the Recycler Ring itself (3). For 15 months, four types of high-frequency, single-ended current buffers (CLC115, AD9620, AD9630, and HFA115) and their associated passive components were rad-tested in the Fermilab Booster. After a dosage of 12 MRad, none of the CLC115, AD9620, or AD9630 circuits had degraded. The quad-packaged CLC115 was selected as the only active component, while metal film resistors and mica capacitors were used whenever possible (4).

A study of the accelerator noise within the 300 kHz-2 MHz passband indicated that the standard solution of coaxial cable may not be best in this case. A balanced, shielded twisted-pair cable with an isolation transformer was chosen for the long runs (150' to 1300') from preamp box to service building racks. Both signal twisted-pair cables were bundled together in a custom cable with another shielded twisted pair for preamp DC power. This "reduced" the total cable to 350,000', reducing the huge installation costs. The cable losses, 0.8 dB/100' @ 1 MHz for the signal cables and 6.2 Ω/1000' for the power cable, were acceptable.

To check for radiation damage and general system operation, test signals can be applied to both channels just before the preamp chip. The amplitude of each test signal is controlled in a scan available on the console application program. The data, however, is not used as a calibration at this time. The signals are created upstairs and coaxially daisy-chained to all preamp boxes in that sector. When test signals are turned off during beam measurement, a DC voltage is turned on to bias on the overvoltage protection diodes in the preamp boxes. This reduces possible noise coupling over the daisy-chain.

Two ion-clearing high voltages, up to ±1000 V, are applied to the detector plates through the preamp box. The HV supplies will be interlocked and separately controlled. Again, a pair of daisy-chains connects all preamp boxes within a sector, but megaohm coupling resistors and shunt capacitors reduce noise coupling concerns.

SERVICE BUILDING ELECTRONICS

Accuracy specifications, schedule, and previous experience were major factors in selecting a method to process the preamp signals. A moderate accuracy in the ±1 mm range was requested, especially within the inner half aperture, over a 44 dB range of beam intensity and cable loss. A high-speed digitizer and digital signal processing were considered because of a similar concurrent project in another group. A more familiar system based on logamps was chosen, however, partially because of the lack of available research and development time.

Logarithmic Amplifiers

The response of an ideal split-plate detector is given by:

$$\frac{A-B}{A+B} = \frac{x}{b} \quad \rightarrow \quad \frac{A}{B} = \frac{1+x/b}{1-x/b}, \tag{2}$$

where A and B are the signal intensities on the two plates, x is position, and b is detector radius. Converting the ratios to decibels, taking the Taylor expansion, and rearranging the first term gives:

$$20\log(A/B) = \frac{40}{\ln 10}\left[\frac{x}{b} + \frac{1}{3}\left(\frac{x}{b}\right)^3 + \frac{1}{5}\left(\frac{x}{b}\right)^5 + ...\right] \rightarrow \frac{x}{b} = \frac{\ln 10}{2}\left(\log A - \log B\right). \tag{3}$$

Implementing the difference of logs can be simpler than difference over sum at many BPM processing frequencies. Recent commercial advances have made possible logarithmic demodulating amplifiers with high dynamic ranges and bandwidths (5). The ideal response of these integrated circuits is given by:

$$V_{out} = k\,\log\left|V_{in}/V_x\right|, \tag{4}$$

where k and V_x determine slope and intercept, respectively. At a CW beam signal frequency f, the resulting output includes baseband and the (typically filtered) higher order even harmonics, each with logarithmic gain compression.

Analog Devices produces several integrated circuits that approximate the ideal log function of Equation 4. The "log nonconformance" error has periodicity and amplitude dependent on the gain of discrete internal gain stages, and this varies among the chip set. This error directly translates into position measurement error and varies according to specific plate intensity ratios. In addition to a log output, these chips have a limiter output for other applications.

The AD640 has 120 MHz bandwidth and 0.3 dB (measured) maximum error, from its 10 dB gain stages. A cascaded pair is required to get 60 dB dynamic range at its higher frequencies. It was used in the 1996 design of the Main Injector 8GeV beamline BPM system to process batches of 53 MHz bunched beam, a similar application to the work investigated at the SSC (6). It has also been used here at low frequencies. The AD606 is a better limiter choice than the AD640, but its logamp output error is larger. Its limiter function has been investigated in an AM/PM circuit, in addition to a 53 MHz synchronous detector with the AD831 active mixer.

The AD608 chip combines an active mixer and a logamp/limiter into one "receiver if subsystem" package. The logamp section has 30 MHz input bandwidth and 0.6 dB (measured) maximum error, from its 16 dB gain stages. A dynamic range of over 60 dB can be achieved with a single chip, for about 10 percent of the price of cascaded AD640s. Figure 2 shows the log nonconformance of several chips, with individual slopes and intercepts normalized.

The low signal bandwidth of Recycler BPM signals and the cost made the AD608 a candidate, but a trick to reduce the log nonconformance enabled its use (6). Taking advantage of the somewhat sinusoidal, 16 dB periodic error function, each input was applied to two separate AD608s. By attenuating the second chip's input by half the error period (8 dB) and adding the outputs, the error is significantly reduced.
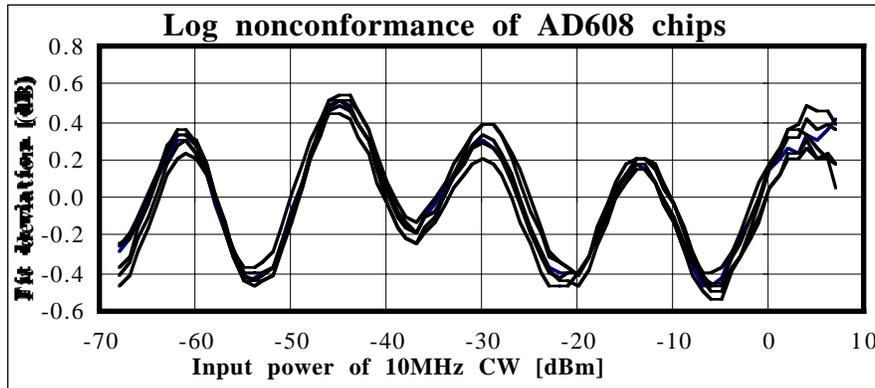
FIGURE 2. Deviation from the ideal logamp response for several AD608 chips.

Analog Processing Module

The balanced inputs to the analog processing module are converted to single-ended with an isolation/balun transformer. These signals are lowpass filtered and applied to the logamps. The four logamp outputs (A_{0dB}, A_{-8dB}, B_{0dB}, B_{-8dB}) are combined into $\log A - \log B$ using AD830s, which perform differencing and summing with excellent common mode rejection and no resistor matching. An external TTL timing signal controls the AD783 track-and-hold, with its 200 ns 0.1% acquisition time and $0.02\ \mu V/\mu s$ droop rate. A final gain and offset stage prepares the held signal for digitization.

The signal at the preamp output is reduced primarily by a back termination and cable attenuation. The range of signal strength at the logamp inputs is estimated between 2 mV and 1V, a good match for the AD608. The exponentially decreasing input (Figure 1) results in a nearly linear output decay (Figure 3), with a slight ripple according to the chip's error characteristic. The difference between two such signals with equal falltimes is ideally flat. Sampling of the position signal occurs early into the decay.
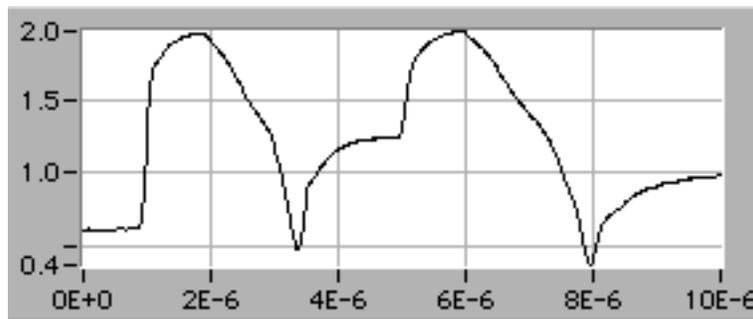
FIGURE 3. Logamp output (33 mV/dB) to preamp output signal in Figure 1.

During testing, response of the analog processing module is scanned over a range of beam positions and intensities (Figure 4). This data is linearly fit against the input

position. The deviation from this fit, converted to millimeters with detector scaling, is the position error (Figure 5).

CAMAC crates were chosen for these modules. The existing (but dedicated) crates saved money and are regularly maintained by the Fermilab Controls Department. The board's power requirements, low frequencies, and its I/O connector scheme also made the CAMAC format possible. Surface mount technology was used to increase density to four BPM channels per board. A single crate at a service building can have up to 20 modules and 80 BPMs, but each location has only 72–76 BPMs.
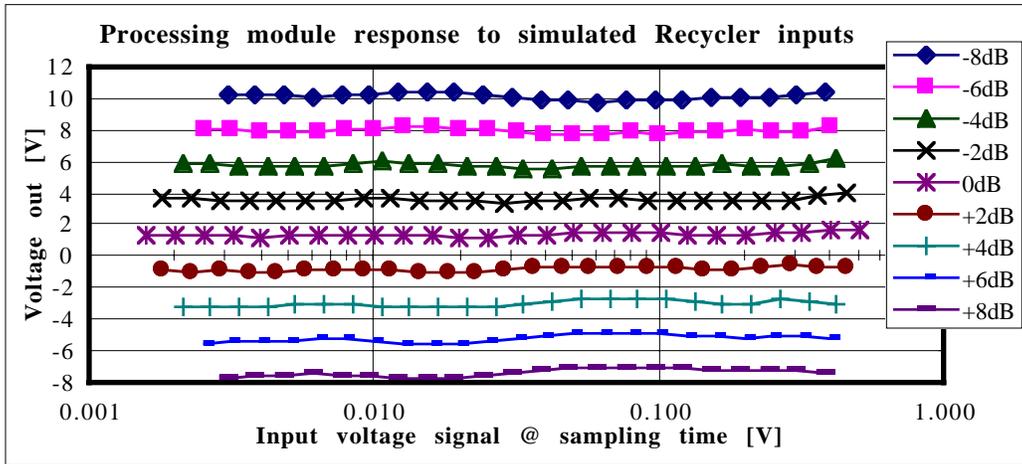
FIGURE 4. Response of an analog processing module to simulated Recycler signal, over a range of beam positions and intensities before offset nulling.
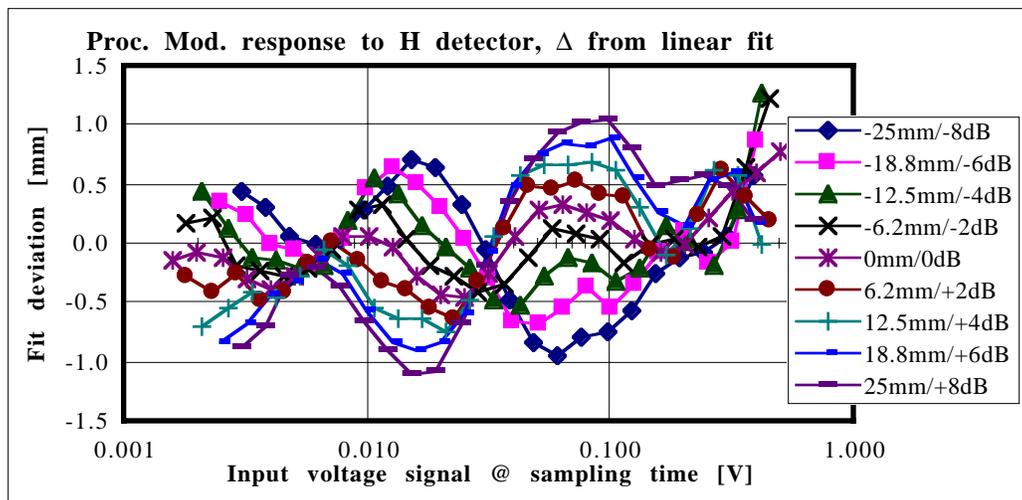
FIGURE 5. Deviation from a linear fit, or position error, for the analog processing module response in Figure 4. Scaling is to the 0.32 dB/mm horizontal detectors. Vertical detector scaling halves this error.

Bundled twisted-pair cables from four preamps are grouped at a racktop distribution PC board into a single, shielded, twist-and-flat ribbon cable, bringing signal inputs to the CAMAC modules. Preamp DC power supply modules connect to the racktop board to distribute power. Another ribbon cable, carrying position signals and external timing signals, connects to a separate transition module. The transition module groups these signals into two 50-pin cables destined for the VME digitizers, and four 50-pin cables from the VME timing signal generators. It also buffers the timing signals and provides test points.

Digital Electronics

A dedicated 3-slot VME crate is home to position signal digitization and processing, timing signal generation, and external communication. The VME processor board is a Motorola MVME162, which has four General Purpose Industry Pack (GPIP) sites. The digitizers are Industry Pack modules (IP320) purchased from Acromag Incorporated. These modules have a 12-bit successive approximation analog-to-digital converter chip (Burr Brown ADS774KE) that is multiplexed to accept 40 single-ended inputs and to digitize them at a rate of up to 100 kHz. Two of the Industry Pack sites are used for digitization, one for horizontal positions and one for vertical. The digitization is triggered either by software or an external TTL signal supplied by the in-house designed timing signal generators.

There are three data acquisition modes. The first mode provides first-turn orbit information for all channels. A beam transfer event will trigger the timing generator to send track-and-hold control signals to the channels, followed by a trigger to the digitizer. The second mode is similar but not tied to the first turn, taking orbits at approximately a 1 kHz rate. It is the default mode. The third mode provides turn-by-turn position of a single horizontal and vertical pair of channels. The mode and the turn-by-turn channels are selected by the user via an ACNET console application program.

The analog processing modules at each service building require TTL track-and-hold control signals. The control signals are created by multichannel timers implemented on Industry Pack modules. On each GPIP resides an ALTERA EPF10K40RC208-3 device, capable of implementing 20 timer channels. The 53 Mhz rf synchronous time base results in 19 ns resolution. Four GPIP modules located on a VME IP carrier module provide 80 track-and-hold signals per service building. All the timers are set high (Track mode) at once after a trigger and a delay. Each timer is set low (Hold mode) at a unique time, since beam signal occurrence varies according to detector location and cable length. For each timer, there is a separate "Hold" time for either antiprotons or counterrotating protons.

The trigger and delay to start the timing signals change according to operating conditions. The trigger can come from a beam transfer event, the Recycler beam synchronous clock, or an external trigger, used primarily to self-trigger during commissioning. The delay has a number of components. Each service building has an adjustable delay to normalize clock event and beam sync occurrence. A systemwide delay, broadcast over the Fermilab MDAT system, tracks the occurrence of the desired rf barrier bucket to be measured. Another common delay is a vernier adjustment of the sampling time within the valid position signal.

The ACNET console application program provides ring orbit and beamline readout for the different acquisition modes. The program also selects measured beam partition, sets timing delays, performs test signal scans, and controls ion clearing voltages.

Outside vendors were used to construct 460 detectors and assemble 460 preamp and 130 analog processing modules. Testing at Fermilab was done with three different Labview-based programs, checking operation within valid ranges and saving data to files.

Commissioning of the Recycler Ring and this system is expected to begin in September 1998.

ACKNOWLEDGMENTS

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